IN THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Claims 1-8 (Canceled)

9. (Currently Amended) A method of manufacturing a semiconductor substrate having shallow trench isolation regions and a device region sandwiched by the shallow trench isolation regions, without using doped silicon oxide containing a melting-temperature-lowering dopant of boron or phosphorus for lowering the melting-temperature of the silicon oxide for performing reflow by doped silicon oxide for planarization, the method comprising:

(a) forming a plurality of grooves on part of a surface of the semiconductor substrate;

(b) depositing oxide films in the grooves by a CVD method using an electrically inert organic silicon source, which does not contain the melting-temperature-lowering dopant;

(c) removing upper parts of the oxide films so as to planarize a surface of a resultant structure until surface areas of the semiconductor substrate are substantially exposed, each of the exposed surface areas of the semiconductor substrate serving as a top surface of a corresponding device region; and

(d) changing ring structure of the oxide films, after said removing, by annealing the semiconductor substrate so as not to melt the oxide films at a substrate temperature which is greater than or equal to 1150℃ but less than or equal to 1350 ℃ so that dislocation density generated in the corresponding device region in a vicinity of the grooves is less than $1\mu m^{-2}$.

10.(Previously Presented) The method of claim 9, wherein the CVD method is any of atmospheric pressure CVD method, low pressure CVD method, plasma CVD method, photo CVD method, and liquid phase CVD method.

11.(Previously Presented) The method of claim 9, wherein the annealing is carried out in any one of reductive gas such as H_2, inert gas such as He, Ne, Ar, Kr, or Xe, O_2, N_2, HCl, CO, and CO_2, or in a gas mixture consisting of any mixture of two kinds of gas selected from these gases.

Claims 12 and 13 (Canceled).

14.(Original) The method of claim 9, wherein each of said grooves has an aspect ratio d/l_{1x} of less than 10, which is defined by a dimensional ratio of a depth d to a width l_{1x} of an opening at a top of each of said grooves.

15.(Original) The method of claim 9, wherein further including arranging said grooves in a cyclic line and space pattern having a line-and-space ratio l_{1x} / l_{2x}, of less than 1.5, and defined as a ratio of minimum space width l_{1x} corresponding to a width of openings of the grooves measured along an axis extending in an x direction to a minimum line width l_{2x} corresponding to a width of a region sandwiched by said grooves, and also measured along said x direction.

Claims 16-23 (Canceled).

24.(Original) The method of claim 15, wherein each of said grooves has an opening having the width l_{1x} and a height l_{1y} measured along a y direction so as to provide a second line-and-space ratio l_{1y} / l_{2y} which is larger than 1.5, with l_{2y} being a space between the grooves and measured along the y direction.

25.(Currently Amended) A method of manufacturing a semiconductor substrate having shallow trench isolation regions and a device region sandwiched by the shallow trench isolation regions, without using doped silicon oxide containing a melting-temperature-lowering dopant of boron or phosphorus for lowering the melting-temperature of the silicon oxide for performing reflow by doped silicon oxide for planarization, the method comprising:

(a) forming a plurality of grooves on part of a surface of the semiconductor substrate;

(b) depositing oxide films in the grooves by a CVD method using an electrically inert organic silicon source, which does not contain the melting-temperature-lowering dopant;

(c) changing ring structure of the oxide films by annealing the semiconductor substrate so as not to melt the oxide films at a substrate temperature which is greater than or equal to 1150℃ but less than or equal to 1350℃ so the dislocation density generated in the semiconductor substrate in a vicinity of the grooves is less than $1 \mu m^{-2}$; and

(d) removing upper parts of the oxide films, after said annealing, so as to planarize a surface of a resultant structure until surface areas of the semiconductor substrate serving as a top surface of a corresponding device region.

26.(Previously Presented) A method of manufacturing a semiconductor substrate having a shallow trench isolation, without using doped silicon oxide containing a melting-

temperature-lowering dopant of boron or phosphorus for lowering the melting-temperature of the silicon oxide for performing reflow by doped silicon oxide for planarization, the method comprising:

(a) forming a plurality of grooves on part of a surface of the semiconductor substrate;

(b) burying oxide films in the grooves by a CVD method using an electrically inert organic silicon source, which does not contain the melting-temperature-lowering dopant; and

(c) changing ring structure of the oxide films by annealing the semiconductor substrate so as not to melt the oxide films at a substrate temperature which is greater than or equal to 1150℃ but less than or equal to 1350℃ so that the oxide films include higher order ring structures higher than 5-fold ring and lower order ring structures lower than 4-fold ring at respective predetermined rates, and an etching rate by ammonium fluoride solution of the oxide films is less than 130 nm/min, which is substantially identical to that of a thermal oxide film.

27.(Currently Amended) A method of manufacturing a semiconductor substrate having a shallow trench isolation, without using doped silicon oxide containing a melting-temperature-lowering dopant of boron or phosphorus for lowering the melting-temperature of the silicon oxide for performing reflow by doped silicon oxide for planarization, the method comprising:

(a) forming a plurality of grooves on part of a surface of the semiconductor substrate;

(b) burying oxide films in the grooves by a CVD method using an electrically inert organic silicon source, which does not contain the melting-temperature-lowering dopant; and

(c) changing ring structure of the oxide films by annealing the semiconductor substrate so as not to melt the oxide films at a substrate temperature which is greater than or equal to 1150℃, but less than or equal to 1350℃ so that the oxide films include higher order ring structures higher than 5-fold ring and lower order ring structures lower than 4-fold ring at respective predetermined rates, the respective predetermined rates of the ring structures are determined according to rates of integrated Raman intensities corresponding to respective ring structures to a total integrated Raman intensity, and the structures are formed to satisfy either of or both conditions that said higher order ring structures are substantially more than 85 % of an overall structure and said lower order ring structures are substantially less than 15 % of the overall structure.

28.(Currently Amended) A method of manufacturing a semiconductor substrate having shallow trench isolation regions and device regions sandwiched by the shallow trench isolation regions, without using doped silicon oxide containing a melting-temperature-lowering dopant of boron or phosphorus for lowering the melting-temperature of the silicon oxide for performing reflow by doped silicon oxide for planarization, the method comprising:

(a) forming a plurality of grooves on part of a surface of the semiconductor substrate;

(b) forming thin thermal oxidation films on the inner walls of the grooves;

(c) depositing oxide films directly on the thin thermal oxidation films by a CVD method using an electrically inert organic silicon source, which does not contain the melting-temperature-lowering dopant;

(d) removing upper parts of the oxide films so as to planarize a surface of a resultant structure until surface areas of the semiconductor substrate are substantially exposed, each of

the exposed surface areas of the semiconductor substrate serving as a top surface of a corresponding device region; and

(e) changing ring structure of the oxide films, after said removing, by annealing the semiconductor substrate so as not to melt the oxide films at a substrate temperature which is greater than or equal to 1150℃ but less than or equal to 1350℃ so that dislocation density generated in the corresponding device region in a vicinity of the grooves is less than $1\mu m^{-2}$.

29.(Currently Amended) A method of manufacturing a semiconductor substrate having a shallow trench isolation regions and device regions sandwiched by the shallow trench isolation regions, without using doped silicon oxide containing a melting-temperature-lowering dopant of boron or phosphorus for lowering the melting-temperature of the silicon oxide for performing reflow by doped silicon oxide for planarization, the method comprising:

(a) forming a plurality of grooves on part of a surface of the semiconductor substrate;

(b) forming thin thermal oxidation films on the inner walls of the grooves;

(c) depositing oxide films directly on the thin thermal oxidation films by a CVD method using an electrically inert organic silicon source, which does not contain the melting-temperature-lowering dopant;

(d) changing ring structure of the oxide films by annealing the semiconductor substrate so as not to melt the oxide films at a substrate temperature which is greater than or equal to 1150℃ but less than or equal to 1350℃ so that dislocation density generated in the semiconductor substrate in a vicinity of the grooves is less than $1\mu m^{-2}$; and

(e) removing upper parts of the oxide films, after said annealing, so as to planarize a surface of a resultant structure until surface areas of the semiconductor substrate are

substantially exposed, each of the exposed surface areas of the semiconductor substrate serving as a top surface of a corresponding device region.

30.(Previously Presented) The method of claim 9, wherein the oxide films are deposited directly on walls of the grooves.

31.(Previously Presented) The method of claim 25, wherein the oxide films are deposited directly on walls of the grooves.

32.(Previously Presented) The method of claim 26, wherein the oxide films are buried directly on walls of the grooves.

33.(Previously Presented) The method of claim 27, wherein the oxide films are buried directly on walls of the grooves.

34.(Previously Presented) The method of claim 28, wherein said thin thermal oxidation films are formed by thermally oxidizing inner walls of the grooves.

35.(Previously Presented) The method of claim 29, wherein said thin thermal oxidation films are formed by thermally oxidizing inner walls of the grooves.

36.(Currently Amended) A method for forming a microelectronic structure, without using doped silicon oxide containing a melting-temperature-lowering dopant of boron or

phosphorus for lowering the melting-temperature of the silicon oxide for performing reflow by doped silicon oxide for planarization, the method comprising:

(a) forming a mask layer on a substrate wherein the mask layer exposes a part of the substrate;

(b) forming a groove in the exposed part of the substrate;

(c) depositing a layer of an insulating film using an electrically inert source, which does not contain the melting-temperature-lowering dopant, so as to fill the groove and cover the mask layer;

(d) changing ring structure of the insulating film by annealing the semiconductor substrate so as not to melt the oxide films at a temperature which is greater than or equal to 1150℃ but less than or equal to 1350℃.

37.(Previously Presented) The method of claim 36, wherein said annealing is performed for a period of time of about 1 hour to about 2 hours.

38.(Previously Presented) The method of claim 36, wherein said annealing is performed for a period of time of about 1 hour.

39.(Previously Presented) The method of claim 36, wherein said annealing is performed in an inert atmosphere.

40.(Previously Presented) The method of claim 36, wherein said annealing is performed in an atmosphere of nitrogen (N_2).

41.(Previously Presented) The method of claim 36, further comprising: planarizing the insulating film so that the substrate is exposed.

42.(Previously Presented) The method of claim 41, wherein said planarizing comprises using a Chemical Dry Etching (CDE) method.

43.(Previously Presented) The method of claim 36, wherein said forming the mask layer comprises forming an oxide layer on the substrate.

44.(Previously Presented) The method of claim 36, wherein said forming the layer of the insulating film comprises forming an oxide layer on inner walls of the groove and depositing an insulating material on the oxide layer to fill the groove.

45.(Previously Presented) The method of claim 44, wherein said depositing the insulating material comprises forming an oxide by a CVD method using the electrically inert source .

46.(Previously Presented) The method of claim 36, wherein the insulating film is deposited directly on walls of the groove.

47 (Canceled)

48.(Previously Presented) The method of claim 36, wherein said groove tapers.

49.(Previously Presented) The method of claim 36, wherein said depositing the layer of the insulating film is configured to deposit the insulating film at a thickness larger than a half of a width of the groove.

50.(Previously Presented) The method of claim 36, wherein said forming the mask is configured to provide a plurality of grooves at a cross sectional view so as to define a SDG region between a couple of the grooves at the cross sectional view.

51.(Previously Presented) The method of claim 50, wherein said SDG region has a width of 0.3 μm, measured between the couple of the grooves.

52.(Previously Presented) The method of claim 50, further comprising:
forming source and drain regions in the SDG region sandwiched by the grooves.

53.(Previously Presented) The method of claim 50, wherein each of the grooves has an aspect ratio d/l_{1x} of less than 10, which is defined by a dimensional ratio of a depth d to a width l_{1x} of an opening at a top of each of the grooves.